We claim:

1. A circuit, comprising:

a first delay line to delay a clock signal by a first amount of time;

a second delay line to delay the clock signal by a second amount of time; and

a signal processor to generate a timing signal from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line.

2. The circuit of claim 1, wherein the timing signal assumes different logical values over a predetermined time period.

3. The circuit of claim 2, wherein the timing signal assumes a first logical value for a longer duration than a second logical value over the time period.

4. The circuit of claim 1, wherein the signal processor includes:

a control circuit to generate an interim timing signal from the clock signal, the interim timing signal having edge transitions which coincide with one of a falling edge and a rising edge of the clock signal; and

a timing circuit to generate the timing signal from the interim timing signal.

5. The circuit of claim 4, wherein the interim timing signal has a period which is substantially twice as long as the period of the clock signal.

6. The circuit of claim 4, wherein the timing circuit sets the first edge of the timing signal based on an edge transition of the delayed clock signal generated by the first delay line, and sets the second edge of the timing signal based on an edge transition of the delayed clock signal generated by the second delay line.

7. The circuit of claim 6, wherein the first edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the delayed clock signal generated by the first delay line, and wherein the second edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the delayed clock signal generated by the second delay line.

8. The circuit of claim 7, wherein the converter further includes:

a first logical transfer circuit to store said logical values of the interim timing signal prior to respective edge transitions of the delayed clock signals generated by the first and second delay lines, said first logical transfer circuit introducing delay that contributes to setting of the first and second edges of the timing signal.

9. The circuit of claim 8, further comprising:

a second logical transfer circuit to output the timing signal based on said logical values stored in the first logical transfer circuit.

10. The circuit of claim 9, wherein the first logical transfer circuit includes a latch and the second logical transfer circuit includes a flip-flop.

11. The circuit of claim 1, further comprising:

a controller to change at least one of the first and second amounts of time in the delay lines to adjust a position of at least a corresponding one of the first and second edges of the timing signal.

12. A signal processing method, comprising:

delaying a clock signal by a first amount to form a first delayed clock signal;

delaying the clock signal by a second amount to form a second delayed clock signal; and

generating a timing signal from the clock signal, the timing signal having a first edge controlled by the first delayed clock signal and a second edge controlled by the second delayed clock signal.

13. The method of claim 12, wherein the timing signal assumes different logical values over a predetermined time period.

14. The method of claim 13, wherein the timing signal assumes a first logical value for a longer duration than a second logical value over the time period.

15. The method of claim 12, wherein generating the clock signal includes:

forming an interim timing signal from the clock signal, the interim timing signal having edge transitions which coincide with one of a falling edge and a rising edge of the clock signal; and

generating the timing signal from the interim timing signal.

16. The method of claim 15, wherein the interim timing signal is periodic with a period which is substantially twice as long as the period of the clock signal.

17. The method of claim 15, wherein generating the timing signal includes:

setting the first edge of the timing signal based on an edge transition of the first delayed clock signal; and

setting the second edge of the timing signal based on an edge transition of the second delayed clock signal.

18. The method of claim 17, wherein the first edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the first delayed clock signal, and wherein the second edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the second delayed clock signal.

19. The method of claim 18, further comprising:

storing said logical values of the interim timing signal in a latch prior to respective edge transitions of the first and second delayed clock signals, said storing introducing delay that contributes to setting of the first and second edges of the timing signal.

20. The method of claim 12, further comprising:

changing at least one of the first and second amounts of delay to adjust a position of at least a corresponding one of the first and second edges of the timing signal.

21. A circuit, comprising:

a switch;

a converter;

a timing circuit to control input of a voltage signal into the converter through the switch, said timing circuit including:

a first delay line to delay a clock signal by a first amount of time,

a second delay line to delay the clock signal by a second amount of time, and

a signal processor to generate a timing signal from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line, wherein different portions of the timing signal independently control switching of the voltage signal into the converter.

22. The circuit of claim 21, wherein a first portion of the timing signal assumes a first logical value for a first period of time and a second portion of the timing signal assumes a second logical value for a second period of time different from the first period of time, and wherein the first logical value of the timing signal connects the voltage signal to the first converter through the switch for the first period of time and the second logical value of the timing signal places the switch in an open position for the second period of time.

23. The circuit of claim 22, wherein the first converter converts a DC level of the voltage signal into a different DC level.

24. A method, comprising:

delaying a clock signal by a first amount to form a first delayed clock signal;

delaying the clock signal by a second amount to form a second delayed clock signal;

generating a timing signal from the clock signal, the timing signal having a first edge controlled by the first delayed clock signal and a second edge controlled by the second delayed clock signal; and

controlling input of a voltage signal into a level converter based on the timing signal, wherein different portions of the timing signal independently control switching of the voltage signal into the level converter.

25. The method of claim 24, wherein a first portion of the timing signal assumes a first logical value for a first period of time and a second portion of the timing signal assumes a second logical value for a second period of time different from the first period of time.

26. The method of claim 25, wherein controlling input of the voltage signal includes:

connecting the voltage signal to the level converter through a switch for the first period of time based on the first logical value of the timing signal; and

placing the switch in an open position for the second period of time based on the second logical value of the timing signal.

27. The method of claim 24, wherein the level converter converts a DC level of the voltage signal into a different DC level.

28. A system, comprising:

a first circuit; and

a second circuit comprising:

(a) a first delay line to delay a clock signal by a first amount of time;

(b) a second delay line to delay the clock signal by a second amount of time; and

(c) a signal processor to generate a timing signal from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line, wherein the timing signal controls operation of the first circuit.

29. The system of claim 28, wherein the timing signal assumes different logical values over a predetermined time period, and wherein each logical value controls a different function of the first circuit.

30. The circuit of claim 28, wherein the first circuit is one of a processor, power supply, graphical interface, chipset, memory, and network interface.